7 JFET Characteristics

7.1 Objectives

- Understanding the basic characteristics of JFETs.

7.2 Basic Description

7.2.a Terminology

JFET : The abbreviation of Junction Field Effect Transistor.

G,D,S : Gate, Drain, Source.

Vp, G_{gs} (Cut-off) : Pinch-off voltage or cutoff voltage for G-S.

I_{DSS} : The saturation current for D-S.

7.2.b Basic Principle

Transistor is a kind of current-control device, and its generating current includes electron flow and hole flow. The transistor is therefore referred to as bipolar junction transistor.

FET is a unipolar device, in which the current of n-channel FET is formed by electron flow and the current of p-channel is formed by hole flow. FET is a kind of voltage-control device. FET can also perform the functions that general transistors (BJT) do, with the only exception that the bias conditions and characteristics are different. Their applications shall thus be chosen in accordance with related advantages and drawbacks. I

The characteristics of FET are listed as follows:

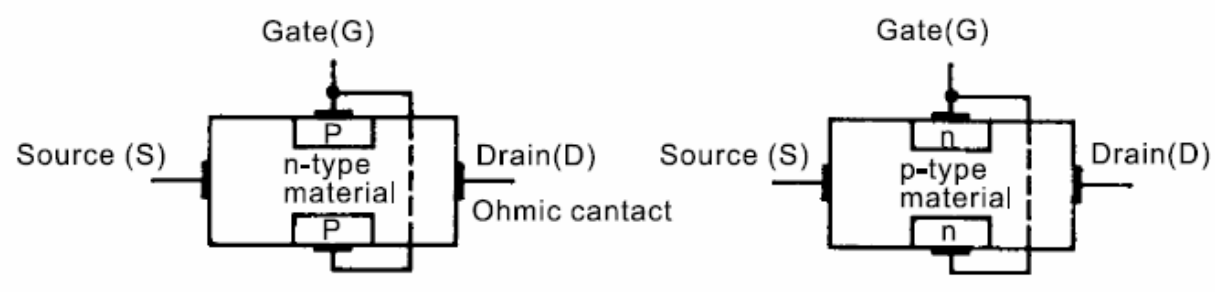
- FET has very high input impedance, typically around 100 MΩ.
- When FET is used as switch, there is no offset voltage.
- FET is relatively independent of radiation, whereas BJT is very sensitive to radiation (β value will be varied).
- Intrinsic noise of FET is lower than BJT, which makes FET suitable for the input stage of low-level amplifier
- During operation the thermal stability of FET is higher than that of BJT.

However, FET also has some drawbacks: comparing with BJT, its product of gain and bandwidth is smaller and it is easier to be damaged by static electricity.

7.2.b.1 Structure and characteristics of JFET

The internal structure of JFET is shown in Fig 7.1. The n-channel JFET is formed by difussing one pair of p-type region into a slab of n-type material. On the contrary, the p-channel JFET is formed by difussing one pair of n-type region into a slab of p-type material. In order to discuss the operation method of JFET, we hereby describe the bias arrangement applied to n-channel JFET as shown in Fig 7.2. The

voltage from power supply Vdd provides the voltage Vds across drain and source so as to generate a current Id from drain to source (in n-channel the electrons actually flow from source to drain, wherein the latter terminal is thus called drain and the direction of conventional current is inverse to the electron flow). Under this situation the drain current is formed by flowing through the channel surrounding the p-type gates. The voltage across gate and source are provided by voltage source Vgg , as shown in Fig 7.2. Because the voltage across gate and source is a reverse bias to the junction of gate-source, no gate current will be generated. The depletion region generated by this gate voltage at sides of channel will narrow the width of this channel, which will increase the resistance between drain and source and further decrease the drain current.



a-) n-channel **b-) p-channel**

Fig. 7.1 – Internal Structure of JFET.

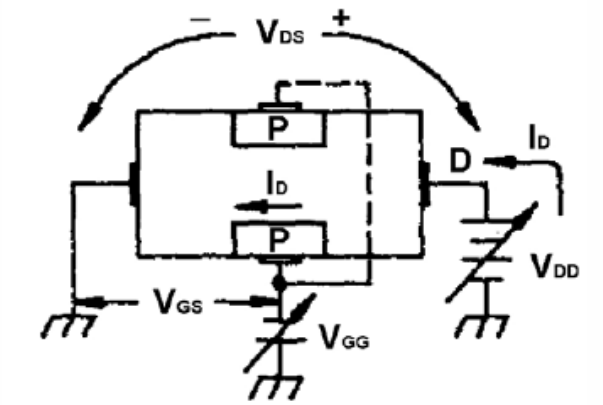
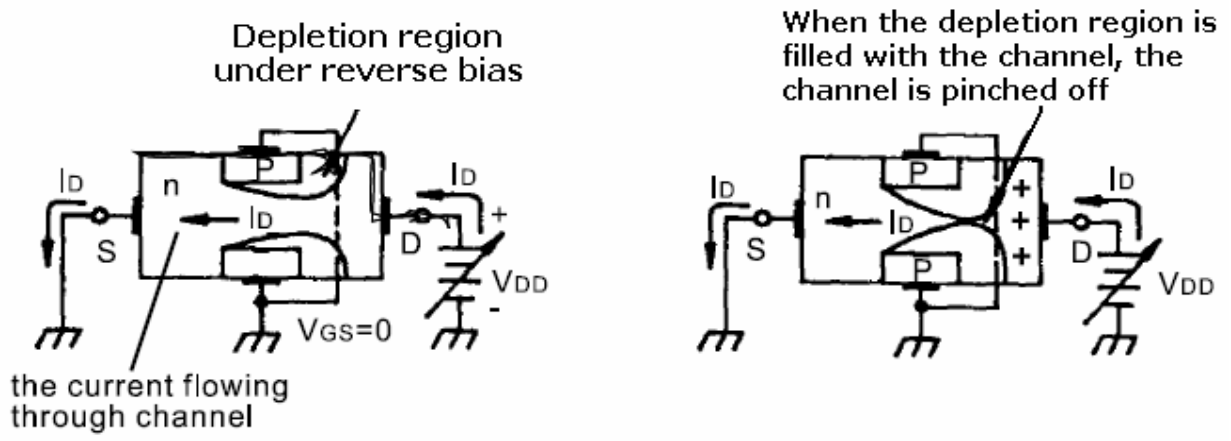


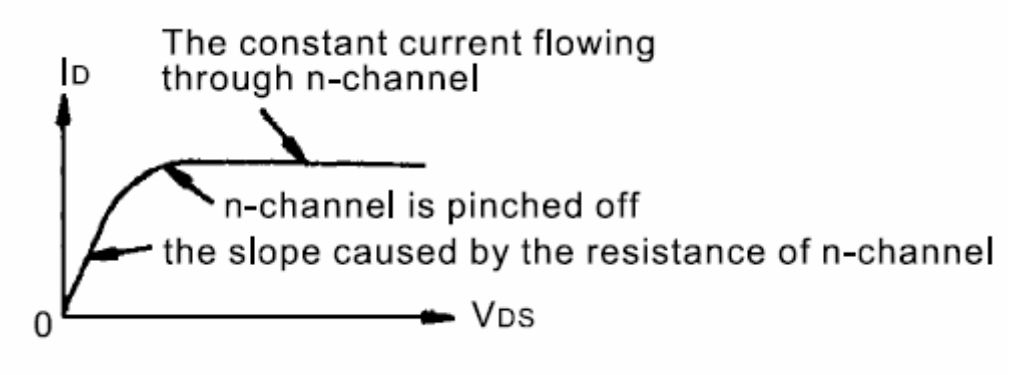
Fig. 7.2 – Basic Operation Method of JFET.

When Vgs = OV, the operation status of FET is shown in Fig 7.3 (a). The voltage drop will be generated by Vdd when a current flows through the n-channel viewed as a small resistor, wherein the potential close to the drain-gate junction is higher than of source-gate junction. The reverse bias applied to P-N junction will thus form the depletion region shown in Fig 7.3 (a). When the voltage source Vdd is increased, the current Id will also be increased correspondingly, which will form the even larger depletion region and will generate the larger resistance between drain and source. If the voltage source Vdd is continuously increased, the depletion region will eventually occupy the full channel, as shown in Fig 7.3 (b). At this time any further increment of Vdd will not increase Id any more (I = V/R, V increases, R increases, I

keeps constant). When Vgs = 0, the relation between Vds and Ids is shown in Fig 7.3 (c). From this figure we can clearly view that Id will be increased with Vds until it maintains at a constant value. This constant value is called Idss, wherein the footnote "ds" means the current from drain to source, and the last "s" means it is under the status that drain-gate are short-circuit (Vgs = 0).



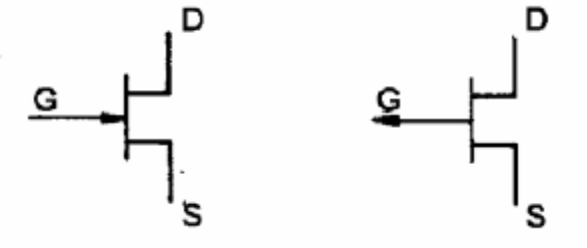
a **b**



C

Fig. 7.3 – The pinch-off effect caused by the channel

7.2.b.2 Circuit Symbols



n-channel JFET **p-channel JFET**

7.2.b.3 Drain-Source Characteristic Curve

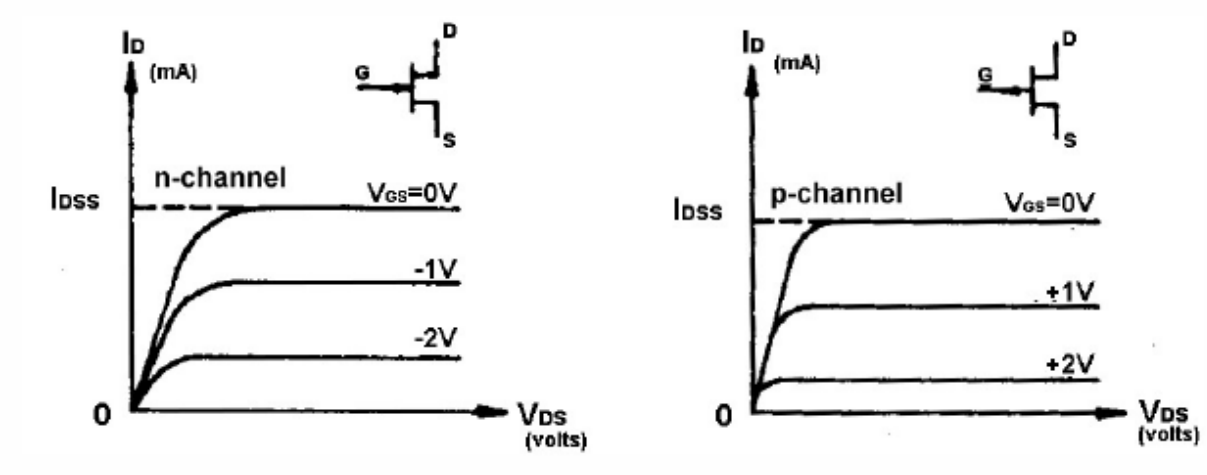


Fig. 7.4 – Drain-Source Characteristic Curve of JFET.

If Vgs is increased (it's more negative to n-channel), depletion will be immediately generated in the channel so that the current required to pinch off the channel will be decreased. The curve corresponding to Vgs = -1V is shown in Fig 7.4 (a). From this result we can find out that the gate voltage functions as a controller capable of decreasing the drain current (at a specific voltage Vds). If Vgs is more positive for p-channel JFET, the drain current will be decreased from Idss (as shown in Fig 7.4 (b)). If Vgs is continuously increased, the drain current will be decreased correspondingly. When Vgs reaches a certain value, the drain current will be decreased to zero and will be independent of the value of Vds. The gate-source voltage at this time is called pinch-off voltage which is usually denoted as Vp or Vgs (cutoff). From Fig 7.4 we can find out that Vp is a negative voltage for n-channel FET and a positive voltage for p-channel FET.

7.2.b.4 Transfer Characteristic Curve

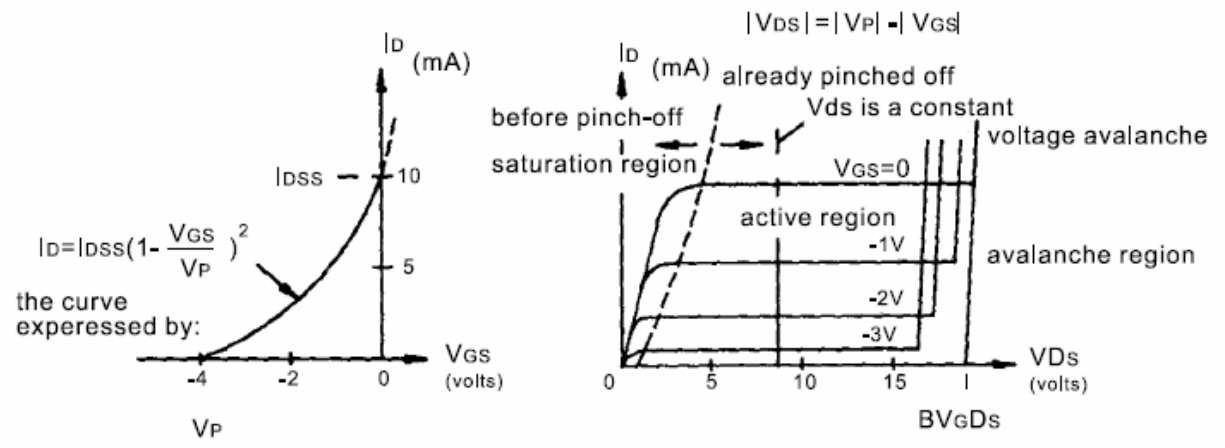


Fig. 7.5 – Transfer and Drain-Source Characteristic Curve for JFET.

Another characteristic curve for JFET is transfer characteristic curve. This is a variation curve of drain current Id corresponding to gate-source voltage Vgs while the drain-source voltage Vds is constant. Two points, Idss and Vp are the most important points in this transfer characteristic curve. When these two points are fixed in the coordinate axes, the remaining points can be looked up from this transfer characteristic curve or can be solved from the formula

$$I_d = I_{dss}(1- V_{gs}/V_p)^2.$$

From this formula,we can calculate

$V_{gs} = 0$, $I_d = I_{dss}$,

$I_d = 0$, $V_{gs} = V_p$.

The design of JFET is typically designed in the middle between Vp and I_{dss} of the transfer curve.

7.3 Experiment Equipments

1. KL- 200 Linear Circuit Lab. Device
2. Experiment Module: KL-23004
3. Experiment Instruments: Oscilloscope, Analog and Digital Multimeter
4. Connection cables and short-circuit clips